WHAT IS CLAIMED IS

1. A semiconductor device, comprising:

a substrate; and

a multilayer interconnection structure formed on said substrate,

said multilayer interconnection structure comprising:

a first guard ring extending continuously in said multilayer interconnection structure along a periphery of said substrate; and

a second guard ring extending continuously in said multilayer interconnection structure along said periphery so as to be encircled by said first guard ring, said second guard ring encircling an interconnection pattern inside said multilayer interconnection structure;

said first and second guard rings being connected with each other mechanically and continuously by a bridging conductor pattern extending continuously in a band form along a region including said first and second guard rings, when viewed in the direction perpendicular to said substrate.

2. The semiconductor device as claimed in claim 1, wherein said bridging conductor pattern does not have any of a gap or an opening.

3. The semiconductor device as claimed in claim 1, wherein said bridging conductor pattern is provided at plural different positions having different heights as measured from a surface of said substrate.

4. The semiconductor device as claimed in claim 1, wherein said bridging conductor pattern is formed in one or more interlayer insulation films in said multilayer interconnection structure.

5. The semiconductor device as claimed in claim 1, wherein said bridging conductor pattern is provided in all of said interlayer insulation films in said multilayer interconnection structure.

6. The semiconductor device as claimed in claim 1, wherein said multilayer interconnection structure has a layered structure in which a plurality of interlayer insulation films each including an interconnection layer corresponding thereto are stacked, and wherein an interconnection layer formed in one interlayer insulation film of said plural interlayer insulation films is connected to an underlying interconnection layer by a via-plug, each of said first and second guard rings having a layered structure identical to that of said multilayer interconnection structure, said bridging conductor pattern being formed at a height identical to that of

the interconnection layer in said interlayer insulation film in which said bridging conductor pattern is formed.

7. A semiconductor device, comprising:

a substrate;

a first multilayer interconnection structure formed on said substrate;

a second multilayer interconnection structure formed on said first multilayer interconnection structure,

said first multilayer interconnection structure comprising: a first guard ring extending continuously in said first multilayer interconnection structure along a periphery of said substrate; and a second guard ring extending continuously in said first multilayer interconnection structure inside along said periphery so as to be encircled by said first guard ring, said second guard ring encircling an interconnection pattern inside said first multilayer interconnection structure,

said second multilayer interconnection structure comprising: a bridging conductor pattern extending in said second multilayer interconnection structure over a band form region continuously, said bridging conductor pattern mechanically connecting said first and second guard rings with each other; and a third guard ring formed on said bridging conductor pattern.

8. The semiconductor device as claimed in

claim 7, wherein said first and second guard rings are connected mechanically with each other by a first conductor pattern extending continuously along the band form region including said first and second guard rings when viewed in a direction perpendicularly to said substrate with a substantially constant height.

9. The semiconductor device as claimed in claim 7, wherein said first multilayer interconnection structure includes an interconnection pattern formed according to a first design rule and the second multilayer interconnection structure includes an interconnection pattern formed by a less stringent second design rule.

10. The semiconductor device as claimed in claim 7, wherein each of said first and second guard rings is formed of stacking of conductor walls extending along said periphery and having a minimum pattern width prescribed by said first design rule, said first and second guard rings being formed with a minimum interval prescribed by said first design rule.

11. The semiconductor device as claimed in claim 7, wherein said first multilayer interconnection structure has a layered structure in which a plurality of interlayer insulation films each including an interconnection layer corresponding thereto and having

a first specific dielectric constant, are stacked, and wherein an interconnection layer formed in an interlayer insulation film of said plurality of interlayer insulation films is connected to an interconnection layer formed in an underlying interlayer insulation film by a via-plug, each of said first and second guard rings having a layered structure identical to that of said first multilayer interconnection structure,

said second multilayer interconnection structure having a layered structure in which a plurality of interlayer insulation films each including an interconnection layer corresponding thereto and having a second specific dielectric constant are stacked and an interconnection layer formed in an interlayer insulation film of said plurality of interlayer insulation films is connected to an interconnection layer formed in an underlying interlayer insulation film by a via-plug, said third guard ring having a layered structure identical to that of said second multilayer interconnection structure, said bridging conductor pattern being formed at a height identical to the height of said interconnection layer in said interlayer insulation film in which said bridging conductor pattern is formed,

said first specific dielectric constant being smaller than said second specific dielectric constant.

12. The semiconductor device as claimed in claim 11, wherein, in said first multilayer interconnection structure, each of said interconnection layers is embedded in a corresponding interlayer insulation film such that a principal surface of said

interconnection layer coincides with a principal surface of said corresponding insulation film substantially.

13. The semiconductor device as claimed in claim 7, wherein said first multilayer interconnection structure uses a film having a specific dielectric constant of less than 3.0 as an interlayer insulation film thereof, and wherein said second multilayer interconnection structure uses a film having a specific dielectric constant of 3.0 or more as an interlayer insulation film thereof.

14. The semiconductor device as claimed in claim 7, wherein said first multilayer interconnection structure uses an organic polymer film as an interlayer insulation film thereof.

15. The semiconductor device as claimed in claim 7, wherein said second multilayer interconnection structure is formed of any of an SiO_2 film or an SiOC film.